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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,978	03/17/2004	Raymond Chow	VP111	3914

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EXAMINER	
GUERTIN, AARON M	
ART UNIT	**PAPER NUMBER**
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,978	CHOW ET AL.	
	Examiner	Art Unit	
	Aaron M. Guertin	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *7-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 18-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/17/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, Claims 1-6 and 18-25 in the reply filed on 11/26/2007 is acknowledged.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 5/09/2007 is being considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,873,332 (Higashi) in view of U.S. Patent No. 5,021,950 (Nishikawa).

5. Regarding claim 1, Higashi teaches of a method for increasing the processing capability of a device, comprising: **requesting access to a module in a display controller** (Fig. 2, (ST201 and ST202)); **processing continuously until notification by the module in the display controller** ([Fig. 2, (ST203)]) ~ ([Column 4 lines 55-61]); **the display controller sends a first signal** (the wait signal generation circuit

generates a time period according to the contents that are to be displayed, once the time period is over, the signal is sent to set off for the next time period) **to a pin** (pins are connections interfacing between components and bus) **when the module is available** (for the second level) ([Column 2, lines 18-43]); **and accessing the module in the display controller after receiving the first signal via the pin** (alternating to the second level) ([Column 2, lines 44-60)]).

Higashi, teaches the limitations of claim 1 above, however, Higashi fails to teach of **wherein a multiplexer in the display controller sends a first signal to a pin.** Nishikawa teaches of a method by multiprocessors for increasing the process capability **wherein a multiplexer in the display controller** (processor (11)) **sends a first signal to a pin** ([Column 1, lines 67-68] and [Column 2, lines 1-19]).

Higashi teaches of a of a method for increasing processing capabilities with a waiting signal to withhold the second time and level of processing until the first time period is complete based on how much data is being processed and displayed in the first level. This is controlled by a module that corresponds to a bus (pins being the connections between the components within the bus that toggle when data is to be moved). Since Nishikawa teaches of a method of multiprocessors corresponding for increasing the processing capabilities that uses multiplexers and arbitration blocks to interface within the bus in order to send signals which allows the use of several processors that continue processing while in an interrupted stage and hold until the next processor transmits its data upon availability (when not busy) of the system ([Column 1, lines 67-68], [Column 2, lines 1-19], and [Column 2, lines 52-67]), it would have been

obvious to combine the teachings of Nishikawa and Higashi. Doing so would have provided the means for increasing processing capabilities by use of a waiting signal with the used of multiplexers and arbitration blocks to allow the a more advanced and a continuous processing of data to between processing and the system to eliminate wasted time processing only during the availability of the system.

6. As per claim 2, Higashi teaches of wherein requesting access to a module in a display controller includes **transmitting a second signal to the module in the display controller** ([Column 1, lines 43-54] and [Column 2, lines 44-60]).

7. Regarding claim 3, Higashi teaches of **wherein processing continuously** (processes the first data and displays data) **until notification by the module** (wait signal alternates to second level and second time) **in the display controller** ([Column 1, lines 43-54] and [Column 2, lines 44-60]). Higashi teaches the limitations of claim 3 above, however Higashi fails to teach wherein the display controller **includes checking the pin in response to the first signal**. Nishikawa teaches of increasing processor capability and also of **checking a pin** (pins being the connections between the components within the bus that toggle when data is to be moved) **in response to the first signal**.

8. As per claim 4, Nishikawa teaches of **wherein processing continuously** ([Column 1, lines 62-66] - processing includes system operations) **until notification by**

the module in the display controller includes selecting a wait signal or a busy signal from the multiplexer to transmit the first signal ([Column 1, lines 67-68] and [Column 2, lines 1-19]).

9. As per claim 5, Nishikawa teaches of **wherein selecting one of the wait signal and the busy signal from the multiplexer includes halting processing** ([Column 1, lines 67-68] and [Column 2, lines 1-19]).

10. Claims 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,021,950 (Nishikawa), in view of U.S. Publication No.: US 2003/0081934 A1 (Kirmuss).

11. Regarding claim 18, Nishikawa teaches of a display controller configured to receive a first signal, comprising: **a plurality of first modules** ([Fig. 2, (33, 45, 27, 25, 23, 29, 47, 21)]) **internal to the controller** ([Fig. 1, (11)]), **the plurality of first modules being capable of accessing a plurality of second modules** ([Fig. 1, (17, 15, 13)]) **external to the controller** ([Fig. 1, (11)]); **a multiplexer** ([Fig. 3, (61, 53, 51)]); **the multiplexer being capable of transmitting a second signal** (Restart Signal) **to a pin by selecting one of a wait signal and a busy signal** (Busy Signal) **in the multiplexer in response to the first signal** (read or write operation accompanying the stop request signal) ([Column 3, lines 38-48] and [Column 4, lines 25-49]); **and a**

connector (bus) **coupled to the multiplexer and the pin, the connector being capable of transmitting the second signal to a source of the first signal** ([Column 3, lines 22-28], [Column 3, lines 38-48], [Column 4, lines 25-49]). Nishikawa teaches the limitations of claim 18 above, however, Nishikawa fails to specifically teach of wherein a multiplexer is **coupled to a plurality of first modules via a combinatorial multiplexer**. Kirmuss discloses of a display controller configured to receive a first signal (Fig. 1a discloses parts 131, 132, and 130 being sensors and programmable controller, wherein signals are sent from sensors and act accordingly to the programmable controller ([0109])) and further of wherein a multiplexer ([Fig. 1, (116)]) is **coupled to a plurality of modules** (151 and 112) **via a combinatorial multiplexer** ([Fig. 1, (110)]). Nishikawa teaches of a method of multiprocessors corresponding for increasing the processing capabilities that uses multiplexers and arbitration blocks to interface within the bus in order to send signals which allows the use of several processors that continue processing while in an interrupted stage and hold until the next processor transmits its data upon availability (when not busy) of the system ([Column 1, lines 67-68], [Column 2, lines 1-19], and [Column 2, lines 52-67]). Since Kirmuss discloses a processing system focused on display control with a plurality of processing modules for data with an emphasis on image and video types of data it would have been obvious to combine the teachings of Nishikawa's display controller components and features with those of Kirmuss. Doing so would provide the means for a more optimal processing system for data that included Nishikawa's continual processing method with busy and restart signals for when the data is being transferred, with Kirmuss's multiple types of

video and imaging processing capabilities and more advanced control of data for user discretion by user interface and programmable controllers.

12. Regarding claim 19, Nishikawa teaches of **wherein the busy signal propagates via the connector** [Column 1, lines 62-68], [Column 2, lines 1-19], and [Column 2, lines 52-67]).

13. Regarding claim 20, Nishikawa teaches of **wherein the first signal** (read or write operation accompanying a stop signal) **is a transmission requesting one of read and write access to the plurality of first modules** (Fig. 2, (23, 21, 33, 29)) ([Column 4, lines 25-49]).

14. Regarding claim 21, Nishikawa teaches of **wherein the second signal** (Restart Signal) **is a transmission from the plurality of first modules** (Fig. 2, (23, 21, 33, 29)) **to the pin indicating the availability of the plurality of first modules for one of read and write access** ([Column 3, lines 21-34], [Column 38-48], and [Column 4, lines 25-49]).

15. As per claim 22, Nishikawa teaches of **wherein a first selector is capable of selecting one of a wait signal and a busy signal in the multiplexer** ([Column 1, lines 67-68] and [Column 2, lines 1-19]).

16. As per claim 23, Kirmuss teaches of **wherein a second selector in the combinatorial multiplexer** (Fig. 1a, (110)) **is capable of selecting a module from the plurality of first modules** ([0100] and [0101]).

17. As per claim 24, Nishikawa teaches of **wherein the source of the first signal is a processor continuously processing** ([Column 1, lines 62-66] - processing includes system operations; [Column 1, lines 67-68] and [Column 2, lines 1-19]).

18. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,873,332 (Higashi) in view of U.S. Patent No. 5,021,950 (Nishikawa) as applied to claims 1-5 and 18-24 above, and further in view of U.S. Patent No. 5,287,471 (Katayose).

19. Regarding claim 6, Higashi and Nishikawa teach the limitations of claims 1-5 above however both Higashi and Nishikawa fail to specifically teach of wherein requesting access to a module in a display controller further includes **providing indirect addressing for communication**. Katayose of a data transfer controller that operates to assist processing operations for a display controller and further wherein indirect addressing is used when transferring the content from the memory to the display ([Column 5, lines 56-61]). Higashi and Nishikawa teach of a of a method for increasing processing capabilities with a waiting signal to withhold the second time and

level of processing until the first time period is complete based on how much data is being processed and displayed in the first level. This is controlled by a module that corresponds to a bus (pins being the connections between the components within the bus that toggle when data is to be moved). Furthermore, teaching of a method of multiprocessors corresponding for increasing the processing capabilities that uses multiplexers and arbitration blocks to interface within the bus in order to send signals which allows the use of several processors that continue processing while in an interrupted stage and hold until the next processor transmits its data upon availability (when not busy) of the system. Since Katayose discloses of operations with a display controller wherein memory and transferring of the processed data using indirect addressing, it would have been obvious for one skilled in the art to have combine the teachings of Higashi and Nishikawa with those of Katayose. Doing so would have provided the means of having the ease of implementation of pointers, and ease of calling subroutines which would not have otherwise been addressable, with the indirect addressing feature provided by Katayose, for the display controller and having the advanced methods of being able to continuously process data though a controller might not be ready to receive the data and then to transport the data upon availability.

20. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,021,950 (Nishikawa) and U.S. Publication No.: US 2003/0081934 A1

(Kirmuss) as applied to claims 18-24 above, and further in view of U.S. Patent No. 5,287,471 (Katayose).

21. Regarding claim 25, Nishikawa and Kirmuss teach the limitations of claims 18-24 above however both Higashi and Nishikawa fail to specifically teach of **wherein the source communicates via indirect addressing**. Katayose of a data transfer controller that operates to assist processing operations for a display controller and further wherein indirect addressing is used when transferring the content from the memory to the display ([Column 5, lines 56-61]). Nishikawa and Kirmuss teach of a method of multiprocessors corresponding for increasing the processing capabilities that uses multiplexers and arbitration blocks to interface within the bus in order to send signals which allows the use of several processors that continue processing while in an interrupted stage and hold until the next processor transmits its data upon availability (when not busy) of the system ([Column 1, lines 67-68], [Column 2, lines 1-19], and [Column 2, lines 52-67]). Furthermore disclosing a processing system focused on display control with a plurality of processing modules for data with an emphasis on image and video types of data. Since Katayose discloses of operations with a display controller wherein memory and transferring of the processed data using indirect addressing, it would have been obvious for one skilled in the art to have combine the teachings of Nishikawa and Kirmuss with those of Katayose. Doing so would have provided the means for a more optimal processing system for data that included Nishikawa's continual processing method with busy and restart signals for when the

data is being transferred, with Kirmuss's multiple types of video and imaging processing capabilities and more advanced control of data for user discretion by user interface and programmable controllers and also of having the ease of implementation of pointers, and ease of calling subroutines which would not have otherwise been addressable, with the indirect addressing feature provided by Katayose, for the display controller and having the advanced methods of being able to continuously process data though a controller might not be ready to receive the data and then to transport the data upon availability.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

23. Brown, (U.S. Patent No. 6,201,739) discloses of a nonvolatile writable memory with preemption pin. This prior art is relevant because the disclosure teaches of wherein suspending or aborting an operation (freeing the processor) allows other operations to be performed (after having notified of the suspension, completion, or abortion of the previous process).

24. Faget, (U.S. Patent No. 5,907,691) discloses of a dual pipelined interconnect. This prior art is relevant because the disclosure teaches of an interface that receives information from a shared input buss that includes status data identifying whether the

information is priority information or not, and from this determination the system halts the processing of the non priority information while sending a signal to resume the processing of the priority information. Finally once this is complete, the resuming of the lower priority processing is then complete.

25. Nilsson, (U.S. Patent No. 6,189,052) discloses of an on-chip I/O processor supporting different protocols having on-chip controller for reading and setting pins, starting timers, and generating interrupts at well defined points of time. This prior art is relevant because it the disclosure teaches of and interface for controlling and communication with peripheral devices, using wait (interrupt) signals at intervals for better management of data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron M. Guertin whose telephone number is 571-270-1547. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao Wu can be reached on 571-272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aaron M. Guertin
Art Unit 2628
January 23, 2008
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